



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE

United States Patent and Trademark Office

Address: COMMISSIONER FOR PATENTS

P.O. Box 1450

Alexandria, Virginia 22313-1450

www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/566,698	05/30/2006	Jens Brandt	S4-03P09159	9692
24131 7590 07/03/2008 LERNER GREENBERG STEMER LLP P O BOX 2480 HOLLYWOOD, FL 33022-2480				
EXAMINER VORTMAN, ANATOLY				
ART UNIT 2835		PAPER NUMBER		
MAIL DATE 07/03/2008		DELIVERY MODE PAPER		

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/566,698

Applicant(s)

BRANDT ET AL.

Examiner

ANATOLY VORTMAN

Art Unit

2835

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 30 May 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 12-23 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 12-23 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on N/A is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/CIS-300)
- 4) ☐ Interview Summary (PTO-413)
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____
- Paper No(s)/Mail Date 02/01/2006

DETAILED ACTION

Drawings

1. The subject matter of this application admits of illustration by a drawing to facilitate understanding of the invention. The drawings are currently not on file in this 371 application. Applicant is required to furnish a drawing under 37 CFR 1.81(c). No new matter may be introduced in the required drawing. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). For examination purposes the drawings from the underlying PCT/EP04/51634 have been referred to.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 12-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over US/2002/0112870 to Kobayashi et al (Kobayashi) in view of EP/0,854,666 to Lochbrunner et al. (Lochbrunner) (both references cited in IDS) and further in view of US/2001-0017766 to Murowaki et al (Murowaki).

4. Regarding claims 12-14, and 21-23, Kobayashi disclosed (Fig. 1) an electronic unit (control device for motor vehicle (see section [0003])), comprising: a printed circuit board (2) having a central region populated with electronic components (see section [0040]), and an edge region adjoining said central region (inherently); a housing (4) enclosing said printed circuit board, said housing having a housing floor (5) and a housing cover (8) connected to said housing floor, said housing floor, when viewed in cross-section, having at least one indentation (Fig. 6) and housing internal lateral sections (52, 53); said central region of said printed circuit board being disposed spaced apart from said housing and said edge region being connected to said housing internal lateral sections via a heat-conducting adhesive layer (9) (Fig. 4) (the adhesive inherently will conduct heat); said housing cover having an edge formed with an annularly continuous projection (84) engaging into a corresponding groove (59) formed in said housing floor, said projection and said groove together forming a groove-and-projection connection and being glued to one another, but did not explicitly stated that the electronic components are disposed on both sides of the circuit board and that the same heat conductive adhesive is used to mount the circuit board to the housing of the electronic unit.

Lochbrunner shows conventionality of placing electronic components on both sides of the circuit board (see last two (2) lines of the translated abstract).

It would have been obvious to a person of the ordinary skill in the relevant art at the time of the invention to dispose the electronic components on both sides of the printed circuit board (2) of Kobayashi device, as taught by Lochbrunner, in order to reduce the required surface area of the printed circuit board, and subsequently, to reduce the size of the device.

Further, Murowaki disclosed that a heat conductive adhesive is used to mount the circuit board to the housing of the electronic device in order to enhance the conduction of heat (see section [0062]).

It would have been obvious to a person of the ordinary skill in the relevant art at the time of the invention to mount the circuit board to the housing of the electronic unit in the device of Kobayashi via a heat conductive adhesive, as taught by Murowaki, in order to reduce the thermal resistance between the circuit board and the housing, thus enhancing the cooling of the Murowaki device. It would have been also obvious to substitute said adhesive (9) in the Kobayashi- Lochbrunner combination, in order to reduce the thermal resistance between the housing cover (8) and the housing floor (5), thus enhancing the cooling of the electronic unit.

Regarding claim 21-23, the method steps recited in the claims are inherently necessitated by the device structure of Kobayashi as modified by Lochbrunner and Murowaki.

Regarding claims 15 and 16, Kobayashi disclosed (Fig. 5) at least one plug connector (3) integrated in said housing cover (8) for electrically connecting said electronic unit, wherein said plug connector (3) includes terminal pins (not labeled) running straight to said printed circuit board (2) and forming direct contact with said printed circuit board.

Regarding claim 17, Kobayashi as modified by Lochbrunner and Murowaki disclosed all, but did not explicitly stated that said terminal pins contact said circuit board via press-in contacts.

Since the technique of using the press-in contacts has been well known and widely used in the relevant arts at the time of the invention to improve upon similar electronic devices, it would have been obvious to a person of the ordinary skill in the art to apply the aforementioned

known technique to interconnect the terminal pins and the printed circuit board in the Kobayashi-Lochbrunner –Murowaki combination. The modification would have yield predictable benefits (i.e. reduced cost and time of the assembly process due to the avoidance of the step of soldering) and would have been obvious to a person of the ordinary skill to try with reasonable expectation of success. *KSR v. Teleflex*, 550 U.S. ___, 127 S. Ct. 1727 (2007).

Regarding claims 18-20, Kobayashi as modified by Lochbrunner disclosed that said edge region is a printed circuit board section running along a large part of an edge of said printed circuit board in an annularly continuous manner (see Fig. 1 of Kobayashi or Lochbrunner), wherein said edge region has first side at least partly populated with the electronic components (see Fig. 1 of Lochbrunner), and a second side connected with said heat-conducting adhesive layer (see Fig. 4 of Kobayashi).

Conclusion

5. The additional prior art made of record on PTO-892 was not relied upon, but is considered pertinent to Applicant's disclosure, because of the teachings of various housings and casings for electronic devices comprising printed circuit boards disposed therein.
6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to ANATOLY VORTMAN whose telephone number is (571)272-2047. The examiner can normally be reached on Monday-Thursday, between 10:00 am and 8:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Jayprakash Gandhi can be reached on 571-272-3740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Anatoly Vortman/
Primary Examiner, Art Unit 2835